A 5-WATT C-BAND FET AMPLIFIER

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ABSTRACT

A GaAs FET amplifier was developed for 5 watts of power output in the 4.4-5.0 GHz band. The amplifier consists of a 1 watt driver module and a 5 watt power booster amplifier containing four FETs in parallel. The six-stage amplifier had a small signal gain of 56 dB, and efficiency of 20%.

Introduction

The power output capability of GaAs FETs has been increasing steadily in the past few years. FETs with a power output of 1-2 watts are now commercially available in C-band and low X-band frequencies. In this paper, we will describe a multi-stage FET amplifier using commercially available FETs with an "improved" four-way power combiner to attain 5 watts of power output in C-band. This amplifier is designed for linear amplification for transmitters in communication systems (4.4-5.0 GHz) and the Microwave Landing System (5.0-5.1 GHz).

The amplifier contains five single FET stages and a power booster stage. The overall gain of the amplifier is 56 dB and power output is 5 watts across the frequency band of 4.4-5.0 GHz with 20% D.C. to R.F. conversion efficiency. The design and performance of the multi-stage driver amplifier and the four-way power-combined booster amplifier are described in the following paragraphs.

Driver Amplifier Design

The driver amplifier is made of five FET stages constructed in modular form with integral isolators. The schematic diagram of the driver amplifier is depicted in Figure 1 with its gain distribution and the power output level of each stage. Figure 2 shows an internal view of the five-stage amplifier consisting of three modules. The input module is a two-stage amplifier designed with 1-micron gate length low-noise FETs. Two intermediate stages are made of power FETs rated at 300 mW and 800 mW, respectively. The output module is a single-stage power amplifier using a 1.5 watt FET. The input circuit for each module is optimized for maximum gain. The output circuit impedance matching is designed along the maximum power output impedance locus (VSWR $\sim$ 3:1) using the design procedure described previously[1]. A bias regulator, designed to operate FETs from unregulated supplies, is included within the amplifier housing. The regulator includes a time-delay network designed to prevent the drain supply from being applied without a proper gate bias.

Figure 3 is a plot of power output vs. frequency at various input levels. The nominal small signal gain of the five-stage amplifier is 50 dB, and its power output at the 1 dB compression point is 1 watt. The saturated power output is 1.4 watts.

Power Booster Amplifier Design

To increase the power output of the amplifier, a power combining circuit is needed. Two widely used circuits for paralleling two transistors in microstrips are the interdigitated parallel line 3 dB coupler[2] and the Wilkinson split-tee power divider[3]. The double-ended balanced amplifier using the 90° hybrid coupler has an additional advantage of presenting a lower input and output VSWR even when the individual amplifier has a high VSWR. High VSWRs result from minimum noise matching, gain equalization matching, or maximum output power matching. The interdigitated parallel line 3 dB coupler, used in the broadband balanced amplifiers, requires a precision circuit etching technique for a tight control of the spacing between microstrip lines. The Wilkinson split-tee power divider was used for power combining in our design because it is less sensitive to fabrication tolerances and has a lower insertion loss than the 3 dB interdigitated coupler. In the conventional split-tee power combiner arrangement[4], the two output ports of the power divider are in phase, and the input VSWR is approximately equal to the VSWR of each individual amplifier. To attain maximum output power and minimum VSWR simultaneously, an extra isolator would be normally required.

The split-tee power dividers in our design contain extra 90° line lengths (Figure 4). In this circuit, the input signal is split into four equal amplitude signals, amplified by four separated FET amplifiers, and combined. The power outputs from the four amplifiers add in phase in the output port since the extra 90° line length in the input circuit of one power-splitter arm is balanced by the same line length in the output of the other arm. The reflected signals due to high VSWRs of the amplifiers, however, are 180° out of phase and absorbed in the 100 ohm isolation resistors. To attain 5 watts of output power, four 1.5 watt FETs are combined in the output booster stage. Figure 5 shows the photograph of the 4-way combiner.

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Each individual amplifier in the power combining circuit was designed for maximum output power along the 3:1 VSWR output impedance locus[1]. The resultant VSWR of the power booster amplifier is reduced to less than 1.5:1 without an isolator. The output of the booster stage is shown in Figure 6. The gain of the booster stage is 6 dB at the output level of 5 watts.

Amplifier Performance

The six-stage amplifier has a nominal small-signal gain of 56 dB and 1 dB gain compression power output of 5 watts. The phase deviation from linearity is within $\pm 10^{o}$ across the 600 MHz bandwidth and is less than $\pm 1^{o}$ over 40 MHz bandwidth. The AM/PM conversion rate is $1\text{-}1.5^{o}$/dB over the input dynamic range of -30 dBm to -17 dBm. The two-tone intermodulation products is -18 dBc at the 5-watt output level. The noise figure of the amplifier is 3.7 dB. The amplifier was driven with a +15 volt DC power supply at 1.6A, and a -15 volt supply at 0.05A. Its total dissipation is 25 watts and the overall efficiency is 20% at 5 watts output.

References

1. W. C. Tsai, "Design of High Power C-Band GaAs FET Amplifiers", Digest of Conference on Circuits, Systems, and Computers, Monterey, California, October, 1977.

2. D. D. Paolino, "Design More Accurate Interdigitated Couplers", Microwave, pp. 34-38, May, 1976.

3. E. J. Wilkinson, "An N-Way Hybrid Power Divider", IRE Trans. on MTT, pp. 116-118, January, 1960.

4. Paul Bura, David Cowan, and Ken Bataharon "High-Linear, Medium-Power, 11 GHz FET Amplifier", ISSCC, Digest of Technical Papers, pp. 158-159, February, 1976.

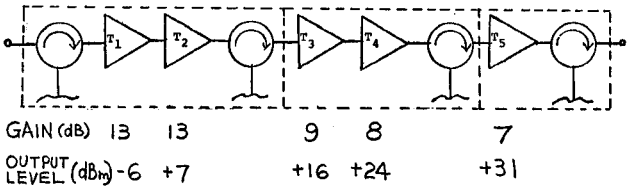

Figure 1 Schematic Diagram of a Multi-Stage Driver Amplifier

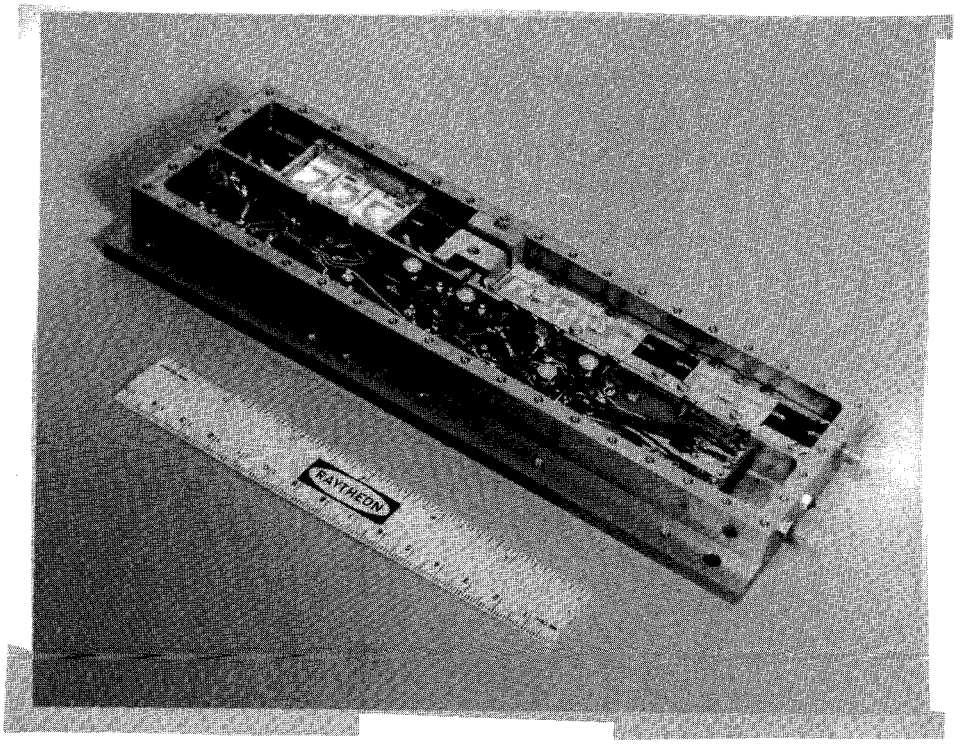

Figure 2 Internal View of Driver Amplifier

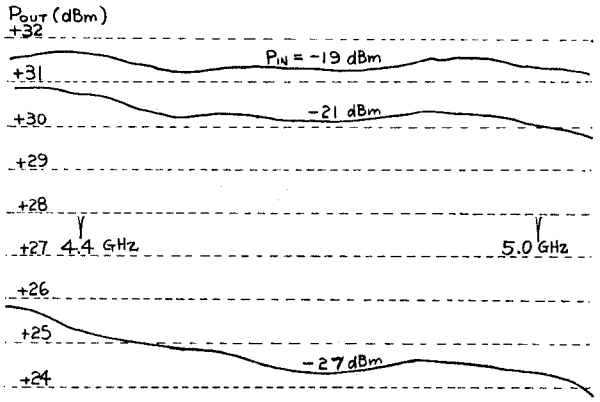

Figure 3 Power Output Response of Driver Amplifier

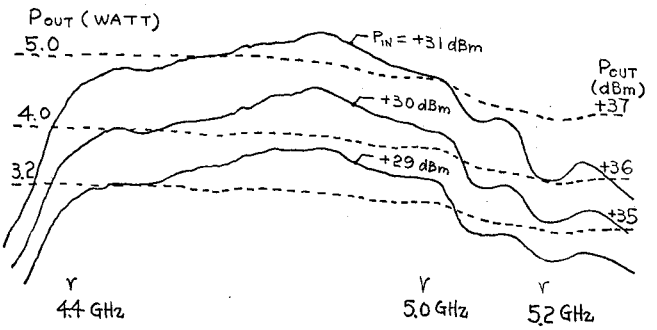

Figure 6 Gain Response of Power Booster Amplifier

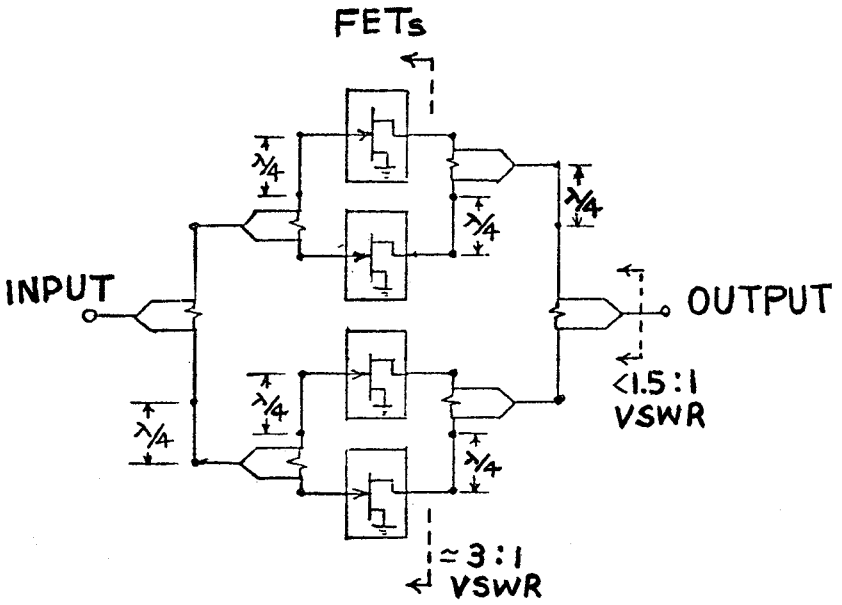

Figure 4 Circuit Schematic of Four-Way Combining Power Booster Amplifier

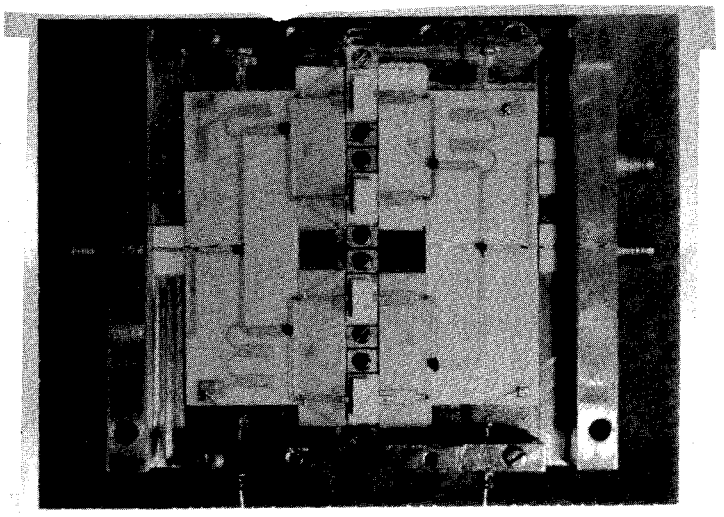

Figure 5 Photograph of Four-Way Combining Power Booster Amplifier